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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,580	07/29/2003	Hiroyuki Abe	108066-00092	4127

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,580	ABE ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,7 and 9-16, 18-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18-28* is/are allowed.

6)☒ Claim(s) *1,4,5,7,9,10 and 12-16* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/12/05 has been entered.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 4, 5, 7, 9, 10 and 12-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Huard et al. (US 2003/0206050).

As to claim 1, Huard et al. discloses in figure 6 a semiconductor integrated circuit comprising: an internal supply voltage generation circuit (14) which generates an internal supply voltage (Vcc) by decreasing an external supply voltage (output of 12), a supply voltage monitoring circuit (64) which monitors a level of the internal supply voltage: a clock control circuit (22, 66) which generates an internal clock (CLK) having a frequency controlled in accordance with an operation speed of the internal circuit and provides the generated internal clock to the internal circuit: and a voltage control circuit (70, 68) which controls the level of the

internal supply voltage generated by the internal supply voltage generation circuit to become a level corresponding to the frequency of the internal clock; wherein the clock control circuit increases the frequency of the internal clock to a first frequency from a second frequency lower than the first frequency, after the supply voltage monitoring circuit detects the level of the internal supply voltage is increased to a level corresponding to the first frequency, and wherein the supply voltage monitoring circuit (64) outputs an internal reset signal (Vnow) when the level monitored by the supply voltage monitoring circuit becomes lower than a predetermined minimum level.

As to claim 4, figure 6 shows that the internal clock is controlled to have a the first frequency, the internal supply voltage is controlled to have a first voltage, and when the internal clock is controlled to have a the second frequency the internal supply voltage is controlled to have a second voltage which is lower than the first voltage (Paragraph [0026-0027]).

As to claims 5 and 7, figure 6 shows that the controlled voltage level of the internal supply voltage is set higher than the minimum voltage level, over which the internal circuit is operational at each frequency of the internal clock.

As to claim 9, figure 6 shows that when the internal supply voltage is controlled to increase from the second voltage to the first voltage, the frequency of the internal clock is controlled to change from the second frequency to the first frequency after increasing the internal supply voltage generated by the internal supply voltage generation circuit to the first voltage is ascertained to complete.

As to claim 10, figure 6 shows that no supply voltage is generated in the standby mode. Therefore, it is inherent that when the internal circuit is controlled to set into standby mode, the

internal supply voltage generation circuit suspends generation of the internal supply voltage.

As to claim 12, figure 6 shows when turning on power, the internal supply voltage is controlled to have a maximum level of the internal supply voltage-level (optional mode).

As to claim 13, figure 6 shows that in accordance with a program executed by a CPU (circuit, not shown, that controls circuit 72) in the internal circuit, the frequency of the internal clock generated by the clock control circuit is controlled, and further the level of the internal supply voltage level generated by the internal supply voltage generation circuit is controlled.

As to claim 14, figure 6 shows that the executed program determines an operation is performed in either a high-speed operation mode (optional mode) or a low-speed operation mode, and when determined as being in the high-speed operation mode, the frequency of the internal clock is controlled to be higher, and also the internal supply voltage is controlled to be higher, while when in the low-speed operation mode (low power mode), the frequency of the internal clock is controlled to be lower, and also the internal supply voltage is controlled to be lower.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huard et al. (US 2003/0206050) in view of Clark et al. (USP 6664775) (previously cited).

Huard et al.'s figure 6 fails to shows a first register which supplies a voltage control signal to the internal supply voltage generation circuit, and a second register which supplies an operation mode signal to the clock control circuit, wherein the CPU modifies data stored in at least either one of the first register and the second register, depending on the executed program. However, Clark et al.'s figure 1 shows circuit using control register (41) to control voltage regulator and clock circuits. Therefore, it would have been obvious to one having ordinary skill in the art to use registers to control Huard et al.'s voltage regulator and clock generator for the purpose of improving the circuit performance. It is also seen as an intended use to use CPU to set value in the newly added registers.

5. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huard et al. (US 2003/0206050) in view of He et al. (USP 6545627).

Huard et al. teaches that circuit 64 can include A/D converter [0028]. Huard et al. fails to teach the detail of the A/D converter. However, he et al.'s teaches an A/D converter with the benefit of less die area and fast conversion time. Therefore, it would have been obvious to one having ordinary skill in the art to use He et al.'s A/D converter for Huard et al.'s sensor 64 for the purpose of saving space and improving circuit speed. Thus, the modified Huard et al.'s figure 6 shows that the supply voltage monitoring circuit has a supply voltage detection register (He et al.'s 130) which stores data indicating the level monitored by the supply voltage monitoring circuit, and the clock control circuit changes the internal clock in accordance with the data stored in the supply voltage detection register.

Allowable Subject Matter

Claims 18-28 are allowed.

Response to Arguments

6. Applicant's arguments have been fully considered but they are not persuasive. Predetermined minimum level may be any level. Paragraph [0028] also teaches that the voltage sensor outputs multi-bit binary signals. It is inherent that the binary signals will turn off at least one element in circuits 66 and 70. Thus, the signal that causes the turn-off is considered as the reset signal.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

October 18, 2005